Enhanced Clock Gating Technique for Power Optimization in SRAM and Sequential Circuit

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Abstract

Low power VLSI designs are having wide variety of application usage in real-time. VLSI circuits are analyzed with various power reduction strategies. Existing approaches are used the clock frequency control, switching activity and scaling factor for power reduction. The glitching problem and clock triggering issues are higher therefore; the proposed work utilized the improved circuit of clock gating technique. In this proposed work, the enhanced clock gating with D-latch model is constructed to obtain the less power consumption. The traditional clock gating technique is improved by adding clock triggering on LATCH circuit and adding buffer circuit between the source and load circuitry to reduce the clock switching issues like gitching and clocking activity. Here the SRAM and sequential counter circuits are designed to utilize the power reduction strategy for improving the performance. This is applicable for various applications in real world and utilizing the FPGA and DSP application specific circuits. Experimental results are analyzed to obtain the power reduction result of SRAM and sequential circuit. Area, power, and delay are obtained the better results as compared with the previous work. Overall, design is performed using Xilinx 14.2 ISE suit.

Keywords: *Enhanced clock gating; D-Latch gating; SRAM; sequential circuit; Area; Delay*

1. Introduction

Power dissipation reduction issue in VLSI circuits plays a wide role for utilizing real-time applications. Power utilization in VLSI circuit as gatelevel exchanging actions are performed with various techniques. Gate level circuit might be used to select different combination of logics related to power utilization. The noise in digital circuit depends on the power utility, temperature, semiconductor property and so on. The power dispersal is the most part because of ground bouncing on the circuit. The lower bound of the power dissipation can be determined to utilizing data move limits of channel [1]. In gate level circuit, diverse mix of legitimate gateways may deliver same circuit yields however unique estimation of power utilization is obtained [2]. By maintaining a strategic distance from the delay at each information of gate logic, logical utility with module is determined. The semiconductor memory is separated into two sorts that are static and dynamic [3]. The static RAM utilizes bipolar or MOS flip-flops and the dynamic circuit use MOSFETs and capacitors that are used to store the information. The SRAM is segmented to preparing arrangement of sensor nodes, which needs to fulfill the low-power necessity also [4]. Major objective is to reduce the power dissipation of VLSI circuits this utilizes many techniques and novel circuit approaches, which are studied in various reviews. Specifically, dissipated power is decreased utilizing various techniques that are voltage scaling, semiconductor scaling and the utilization of rest semiconductors. The 6T SRAM cell is to keep up the circuit execution and energy productivity with complex design. DFF with large register circuits on VLSI module mostly preferred the clock gating technique to reduce the leakage power [5]. Power dissipation reduction technique done with clock triggering strategy, gated clock generation with switching pulses, and synchronous clock generation circuit [6]. Power utilization is significantly expanding for Static Random Access Memory Field Programmable Gate Arrays along these lines lower power FPGA hardware and new CAD apparatuses are required. Clock-gating approaches have been applied in low force FPGA plans with just minor achievement in diminishing the complete normal force utilization [7]. The clock-gating strategy depends on the fractional reconfiguration and topological adjustments [8]. The arrangement depends on the powerful incomplete reconfiguration of the design memory outlines identified with the clock directing assets. D flip-flop utilizes tree-based clock drivers with gating to significantly decrease the stacking on dynamic clock drivers. Furthermore, D flip-flops are utilized to lessen the clock spikes and, in this manner, diminish the power utilization on the clock signal [9]. Design contains DFF to control the conveyance of the neighborhood clock signal "CLK "to the memory, and the "Lock signals along the way passing the worldwide clock source to the nearby clock signal are dynamic [10]. The yield of DFF and worldwide clock feeds to AND based RTL circuit, which produce neighborhood clock signal for memory [11]. Power utilization is drastically expanding for SRAM-FPGAs, thusly lower power FPGA hardware and new CAD devices are required. Clock-gating philosophies have been applied in low power FPGA with just minor accomplishment in diminishing the all-out power utilization [12]. The clock-gating method depends on inner halfway reconfiguration and topological changes. The arrangement depends on the powerful incomplete reconfiguration of the setup memory outlines identified with the clock steering assets [13].

The exchanging movement of the circuits can be utilized to locate the normal power scattered which thus helps in examining the speed performance. The exchanging movement can be restricted in VLSI plan by utilizing a method called check gating in simultaneous circuits by cutting the inactive patterns of flip flop [14]. Clock gating is the technique for adding additional rationale to infer a gated clock which is taken care of into the DFF.

Delay Minimization and Power Minimization are two significant targets in the plan of optimal circuits [15]. Here the retiming is a viable method of postpone improvement of successive circuits. This depicts a calculation in RTL that discovers least spreading over tree for associated VLSI. The Bellmanford calculation is used at that point of examining the prim approach to focus on the synchronous circuitry [7]. Clock gating is acknowledged as the power advanced procedure as it decreases the power at framework level, RTL and gate level. More significant levels of advancements are accomplished more in RTL level than gate level, where tasks are completed in register blocks as restricted on logical gate circuit [16]. The fundamental point of the clock gating strategy is to remove the clock during the inactive patterns of flip flop [17]. Clock gating procedure is executed for three diverse cell types: 1) Latch based cell, 2) Flip-flop based cell, 3) Gate based cell. The drawback is that, for the positive edge set off counter when empower signal goes from 1 to 0 and when the clock is at rising edge, a glitch happens on account of the more prominent falling time span of empower signal [18] and [19]. The yield acquired is mistaken, in view of the previously mentioned reason. Any risk that happens when empower is equivalent to one is straightforwardly engraved on to the GCLK this is a precarious conduct of the circuit [20]. In this proposed work, the SRAM and sequential circuits are designed to utilize the improved clock gating technique for reducing the leakage power while performing simulation and synthesis. Latch based approach performed with DFF and logics are triggered using clock switching activity. Here the performance is designed to get the better performances of area, delay and power. Here static and dynamic power reduction is done effectively to achieve the better results than existing work.

This paper summarized as follows. Section II describes the various reviews related to the power optimization in VLSI circuits. Section III provides the proposed logic with constructive algorithms and novel designs. Section IV presents the results and discussion. Finally, section V concluded with the proposed logic and future enhancement.

2. Literature Survey

Zamin Ali Khan, et al. (2011) [8] has presented the power consumed VLSI design with power optimization approach, which utilized the genetic algorithm. Booth multiplier VLSI design is constructed to test the power by triggering gated switching logic. Here the GA is used to find out the different combination of gates logic onto the power estimation to determine the fitness value; these consequently reduce the power. Benchmark ISCAS-89 circuit is used and performance analysis depends on the gated logics and power consumption on that circuit. Physical design of VLSI circuit utilized the chip analysis and optimization using GA.

Bo-Cheng C Lai, and Jiun-Liang L, (2017) [2] has presented the multiport memory logic on the RAM design with FPGA implementations. The use of Block RAMs (BRAMs) is a basic execution factor for multiported memory plans on FPGAs. Not exclusively does the exorbitant request on BRAMs block the utilization of BRAMs from different parts of a plan, however the complex steering among BRAMs and interconnection likewise restricts the frequency range. This presents a shiny new viewpoint and a more proficient method of utilizing a regular two peruses one compose memory as a 2R1W/4R memory. By abusing the 2R1W/4R as the structure block, this presents a various leveled plan of 4R1W memory that requires 25% less BRAMs than the past methodology of copying the 2R1W module. Recollections with more read/compose ports can be reached out from the proposed 2R1W/4R memory and the various leveled 4R1W memory.

Nandita S, et al. (2015) [4] has presented the clock gating technique on VLSI circuits for power reduction strategy. The framework is a coordination of fundamental structure contains sensor framework, control units into existing power frameworks which could be actualized as Silicon on Chip (SoC) in VLSI circuits. VLSI circuits can be both sequential and combinational. In consecutive circuits, the clock is the significant wellspring of dynamic power utilization. The method of clock gating is utilized to lessen the clock power utilization by removing the inactive clock cycles. VHDL-based strategy, to embed the clock gating circuit and furthermore the unique power because of this is assessed.

C Ashok Kumar, et al. (2020) [1] has presented the loss minimization strategy of VLSI circuits to analyze the power. The solitary chip planned to reduce low territory frameworks for bringing more proficient gadgets, which are more modest in size. Circuit produced at a very high rate and they devour a space parcel more than they used. The premier worry of VLSI engineers was Area, power performance and Cost. Power has consistently been an optional concern. Latest thing has given more weight to Area, Power and Delay because of versatile specialized gadgets. The high velocity calculation gadgets with complex usefulness are a developing pattern which is request to low power utilization.

Sreenivasulu, et al. (2016) [13] has presented the optimized sequential circuit to reduce the power leakage by multi threshold CMOS circuitry. This method designed to gives lower leakage current and offers upgraded speed. It utilizes low edge voltage gadgets for low leakage and high limit voltage segments as rest semiconductors. These rest semiconductors are sufficient to disconnect the rationale modules from the stock, ground to lessen the spillage current. Furthermore, the most un-conceivable time for turn ON state in a circuit is essential worries for power utilization.

Xuan-Thuan N, et al. (2019) [3] has proposed the RAM based content addressable memory architecture on FPGA using hierarchical partitioning approach. In the clock cycle, the update phase of an RAM-based content-addressable-memory consistently endures high idleness. Two essential drivers of such inactivity include: (1) the mandatory eradicating stage alongside the composing stage and (2) the significant distinction in information width between the RAM-based CAM and the advanced frameworks. The design of RAM-based twofold CAM updates the low latency. A few RCAMs, whose information width goes from 8 to 64 bits, were incorporated into a 256-bit framework for the assessment.

Priya Singh and Ravi Goel, (2014) [7] has presented the comprehensive study of power optimization technique in sequential circuit. Here the clock gating is performed to improve the result. Low power VLSI circuit is the most basic issues in the present ASIC plan, as the element size is downsized and there is a pressing requirement for power advancement. Clock gating is perhaps the most rich and exemplary methods for decrease of dynamic influence, significant factor in all-out power utilization of any VLSI circuit. Clock gating procedure empowers saving of electrical power utilized by PC processors. It guarantees power saving by turning on a practical logic block clock, yet just when required. The survey of existing clock gating procedures and its focal points furthermore, impediments with a demo of D flip lemon and 4-bit Pseudo Random Binary Sequence Generator.

A Jagadeeswaran, et al. (2012) [14] has presented the optimized power level based sequential pulse triggering approach. Flip-flops are the significant storge components in all SOC's. They oblige the majority of the power that has been applied to the chip. Flip-flop is quite possibly the power utilization parts. It is essential to decrease the leakage power in both clock circulation and flip-flops. The power delay is principally because of the clock delays. The deferral of the flip-flop ought to be limited for effective usage. This venture moves around in supplanting regular expert slave based on D-FF to a pulse set off flip flop which goes about as a recognition substitute for low power applications. In this, semiconductor sizes and heartbeat age circuit can be further diminished for power saving. Here UMC CMOS 180 nm innovation is use in SPICE device to plane for the structure.

3. Proposed Method

The proposed design of SRAM and sequential counter circuit is used for analyzing the power by using improved clock gating technique. Here the Static Random Access Memory circuit is designed with improved clock gating technique using D-latch based buffer circuitry of gated clock generation to reduce the power dissipation and the counter circuit of sequential logic is designed with improved clock gating technique. The input enabled logic is performed on the register circuits and it is integrated with the improved clock gating technique. In this, the clock and enable signal applied on the gated clock generation module using D-Latch circuit and it is enabled with the AND logic. Based on the triggering state of the clock switching, the gated clock is generated to the SRAM and sequential counter circuits. When the circuit is in idle condition, the clock switching state occurs with triggering problem this causes increased leakage. Therefore, the clock gated switching control-based logic is designed to utilize the SRAM and sequential counter logic circuit with improved clock gating technique. The proposed block diagram of power reducing technique of SRAM and sequential circuits are using the improved clock gating technique is given in Figure 1.

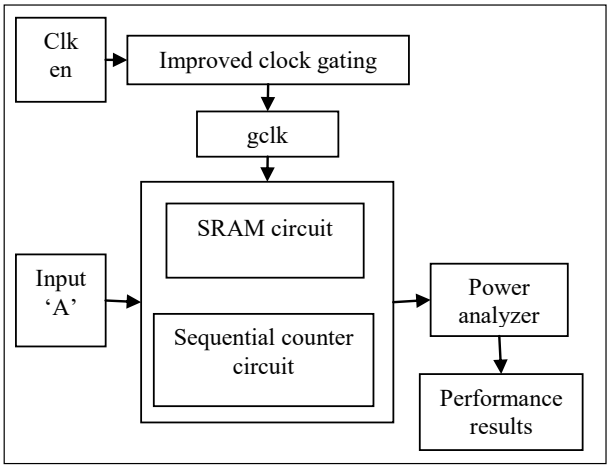

Fig. 1. Proposed block diagram of power optimized SRAM and sequential circuits

The VLSI circuit optimization involved with various technique for improving the performance. By changing the width and length of the transistor, the minimum impact is possible on the VLSI layout circuit. While connecting source and load impedance, the buffer is used to reducing the number processing stages.

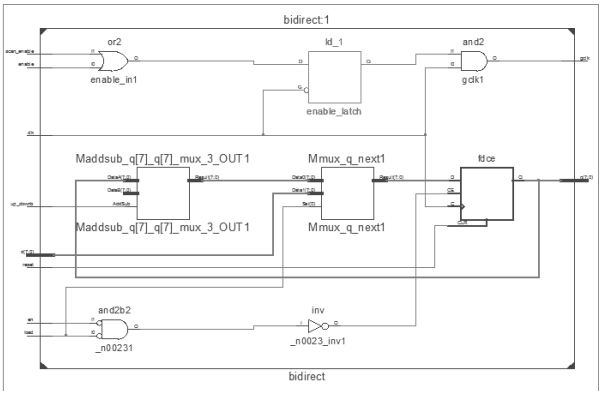

Fig. 2. RTL view of Bidirectional counter with Improved Clock Gating Technique

The RTL schematic of Bidirectional counter circuit is shown in Figure 2. The load decoupling is also helpful for reducing the critical path on circuitry. By strengthening the switching activity, the clock signal variation may get better computation. The static power dissipation of CMOS circuit is reduced by capacitance utilization with better transition activity and the pre-charging the higher capacitance to improve the speed.

3.1 SRAM Circuit

Synchronous RAM is designed with the improved logic of gated clock generation circuit to reduce the power leakage. D Latch registry with level delicates the positive lock passes contribution to yield on high stage, hold time on low enable states. Here the positive register tests on rising edge with sample input and the edge triggering is performed with the flip flops. Static power optimization with clock gated signal generation triggers the logic by switching activity and adding of BUFF logic on gclk. Here the Static power of RAM is controlled and optimized the power with effective utilization.

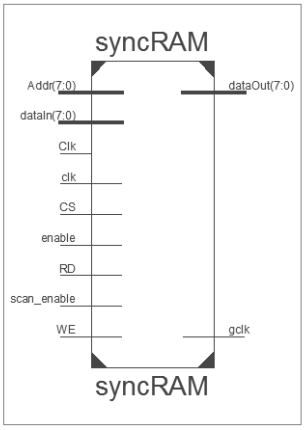

Fig. 3. SRAM circuit RTL schematic

SRAM logic structure is designed to utilize the clock gating approach with RTL view (Figure 3). The clock gating strategy has been created to evade leakage power. When the framework is inactive, the clock switching timing of clock gating is TURN OFF. Explicitly for flip-flops, clock gating implies debilitating the clock signal when the info information doesn't change away the information. It may be applied from the framework level where the whole useful unit can be specifically set into rest mode, or from the sequential circuit level where a few bits of the circuit are in rest mode while the rest of the logic blocks are working. In any case, Clock gating doesn't come free of charge. Additional logics and interconnects are needed to produce the clock empowering signals.

3.2 Sequential Counter Circuit

Sequential counter circuit with bidirectional logic designed with the improved clock gating technique to reduce the power leakage. Here the RTL gate level performance is used for the gated clock circuits to improve the performance. Register with BUFFER utility on D-FF is shown in RTL view (Figure 4).

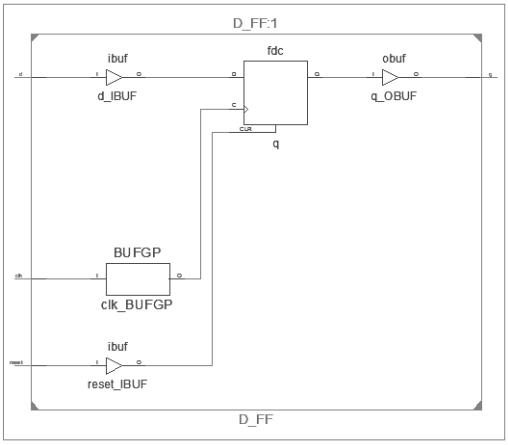

Fig. 4. RTL view of BUFF added D-FF

Power consumption techniques mainly focus the static and dynamic to improve the performance of VLSI circuits. Aside from this short out and leakage assumes a crucial part in fixing the general energy utilization in a circuit. Static power is because of the quantity of intelligent a part utilized in the module and dynamic happens as aftereffect of number of transient states in the logics. Short circuit flows additionally happen in this situation of when both NMOS and PMOS semiconductors are in ON active state. Capacitive activity prompts dynamic energy utilization, which is most moving issue to bargain with as exchanging movement is high in consecutive circuits. If the circuit allows for timing logic with switching activity, the clock edges are reducing its existence on precharging state of capacitance.

3.3 Modified Clock Gating Technique

At the point when the present and next condition of the D flip failure is noticed, it is seen that when two nonstop information sources are indistinguishable, the D flip failure gives a similar incentive as yield. The clock cycle that is taken care of into the D flip lemon when the yield doesn't shift is named as inactive clock cycles. To eliminate these, at the point when the flip lemon are of various qualities the EXOR entryway passes a yield 1 which is given as a yield to the AND entryway alongside a clock beat gave to the flip lemon for additional exchanging movement that happens during various patterns of the clock beats.

$$Pd = Cs\left(Vcc\right)^2 f_{clk}$$

Where the cumulative value of switching clock is denoted as Cs and f_clk mentioned the frequency of clocking to reduce the dynamic power 'Pd' and Vcc denoted as power supply utility to the module.

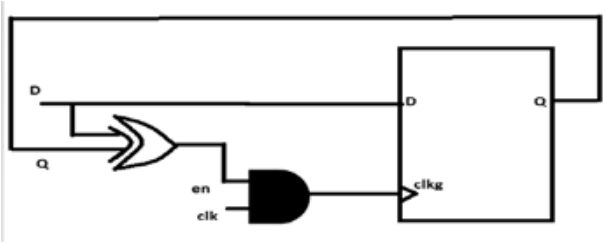

Fig. 5. Block diagram of improved clock gating with D-FF

The Clock gating wit DFF is given in the Figure 5. Setup time and hold time are continually influenced by their contributions as long as empower signal is affirmed. They are empowered, their substance changes promptly when their sources of info change. Flip-flops, then again, have their content change just either at the rising or falling edge of the empower signal. This empower signal is normally the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remaining parts steady even.

4. Results and Discussion

Thus, the design model of SRAM and sequential logic of counter circuit is effective utilization. Modification in clock gating technique reduces the leakage power than traditional approaches. The module comprises of one 8-input combinational logic-into table with four devoted registers and is viewed as a major structure of FPGA block.

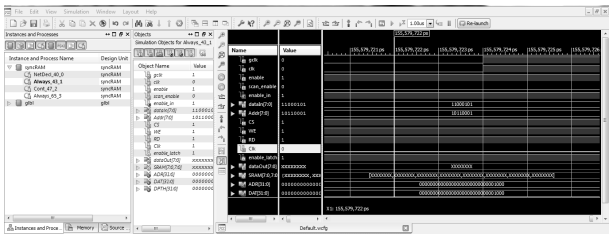

Fig. 6. Simulation result of SRAM circuit

The simulation result of SRAM is shown in Figure 6. Here the gated clock is generated and determines the better utility of performance. The –bit utilization memory is constructed to improve the synchronous logics and it is clock gating is improved the performance of area and delay utility. Here the Tables 1 and 2 show the results of area and delay.

Tab. 1. Area utility of SRAM logic with power optimization strategy

SRAM-Device utilization Summary			
Slice Logic Utilization	**Used**	**Availa-ble**	**Utilization**
Slice Registers	9	93,120	1%
Slice LUTs	6	46,560	1%
Number used as logic	2	46,560	1%
Number used as Memory	4	16,720	1%
Number of occupied Slices	3	11,640	1%
Number with an unused Flip Flop	1	6	16%
No. of fully used LUT-FF pairs	5	6	83%
slice register sites lost to control set restrictions	7	93,120	1%
Bonded IOBs	27	240	11%
BUFG/BUFGCTRLs	2	32	6%

Tab. 2. Delay report

Parameters of delay	Value
Minimum period:	1.257ns
Input arrival time before clock with maximum delay utility	1.324ns
Output required time after clock –maximum reach	1.148ns
path delay - gclk	0.935ns
Clock period	1.257ns
Net delay	0.533ns

The power analysis is the major concern in proposed logic, which utilizes the better utilization on the synchronous RAM with XPower Analyzer tool in Xilinx ISE. Both Static and dynamic power is analyzed with the voltage and current utility, which is shown in Figure 7. When the register activity is TURN OFF, the input data need to register the gated clock and clock gets OFF state. The enable and clock applied on the register block, this is the enable clock gating signal.

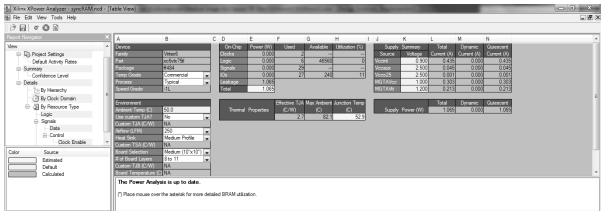

Fig. 7. XPower analyzer result of SRAM

Sequential circuit power reduction is determined the power, area and delay. The ISim result of sequential logic with bidirectional counter is designed and it is shown in Figure 8.

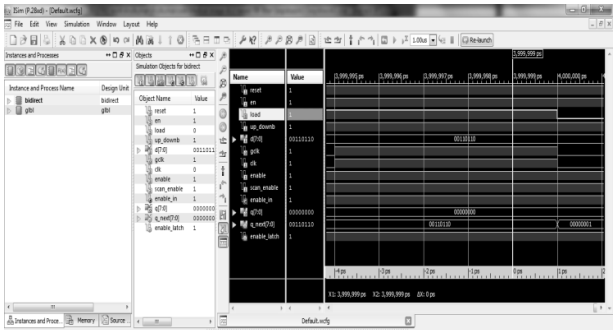

Fig. 8. Simulation result of Bidirectional counter with power optimal strategy

Tab. 3. Device utilization of bidirectional-counter circuit

Device Utilization Summary			
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	9	93,120	1%
Number of Slice LUTs	11	46,560	1%
Number used as logic	11	46,560	1%
Number used as Memory	0	16,720	0%
Number of occupied Slices	5	11,640	1%
Number with an unused Flip Flop	2	11	18%
Number with an unused LUT	0	11	0%
Number of fully used LUT-FF pairs	9	11	81%
Number of slice register sites lost to control set restrictions	7	93,120	1%
Number of bonded IOBs	24	240	10%
Number of BUFG/BUFGCTRLs	1	32	3%

Device utilization summary determines the utility of area, which is given in Table 3. Various delays like path delay, net delay and gate delays are analyzed and it is given in Table 4.

Tab. 4. Delay report of sequential circuit

Parameter	Value
gclk	5.859ns
Clk	1.765ns
input arrival time before clock	1.551ns
Maximum output required time after clock	1.148ns
Maximum combinational path delay	0.935ns
Net delay	1.244ns

Bidirectional counter circuit uses the improved clock gating technique for power analysis, which is shown in Figure 9. Shifting and DFF register utilities are the major logic block of RTL view. Clock pair shared flip-flop based logic, low-swing DFF based logic and gated model of SRAM designs are compared to the proposed logic and it achieves the best result for proposed power reduction technique, which are shown in Table 5.

Fig. 9. XPower analyzer report of Sequential circuit

Tab. 5. Comparison results

Experiment	Power (W) [7]	Delay(ns) [21]
4-Bit Counter(no CG)	22.96	72
4-Bit Counter(with CG)	17.93	49
D flip flop (no CG)	14.299	52
D Flip flop (with CG)	14.202	68
PRBS (no CG)	13.911	112
PRBS (with CG)	12.5	10
Proposed power reduction logic	1.065	6

As one of the most highly desired VLSI design fields, power consumption has grown to become one of the central study areas. Based on the connection between the triggering transition of the clock and the present and the next state function of the flip flop, the clock gating method that has been suggested would gate clocks.

In latch-based clock gating procedure, a sensitive latch is utilized as the control component, to control the Enable pin, that is taken care of to the "AND" "OR" gate level for gating the clock signal. This latch is permitted to mirror the difference in Enable pin. The clock holds the estimation of empower signal from the dynamic edge of the clock till the idle edge of the clock. In the event that the "AND" is utilized for circuits working on certain edge of clock pulse. Therefore, the proposed clock gating based SRAM and Sequential circuit improves the result of area, delay and power than existing work.

5. Conclusion

Thus, it concludes that the design logic of SRAM and sequential counter circuit is improved the performance using improved clock gating technique. Here the power reduction strategy is performed with D-Latch based clock switching with triggering of RTL module in improved clock gating technique. The consequence of this kind of clock gating procedure on a D flip failure is as appeared. Power improvement, generally consigned to the combination, and situation and directing stages, has climbed to the System level also, RTL. HDL can thus utilize clock gating to turn off idle segments of the plan and decrease generally speaking dynamic power utilization. Thus, the RTL view of gate level examination determines the better result of SRAM and sequential Bidirectional counter circuit using improved clock gating approach. In future, the work may extend with the voltage limiting and managing approach for power reduction.

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